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(54) PRODUCTION METHOD OF III NITRIDE COMPOUND SEMICONDUCTOR SUBSTRATE AND SEMICONDUCTOR DEVICE

(57) A GaN layer 31 is subjected to etching, so as to form an island-like structure having, for example, a dot, stripe, or grid shape, thereby providing a trench/mesa structure including mesas and trenches whose bottoms sink into the surface of a substrate base 1. Subsequently, a GaN layer 32 is lateral-epitaxially grown with the top surfaces of the mesas and sidewalls of the trenches serving as nuclei, to thereby fill upper portions of the trenches (depressions of the substrate base 1), and then epitaxial growth is effected in the vertical direction. In this case, propagation of threading dislocations contained in the GaN layer 31 can be prevented in the upper portion of the GaN layer 32 that is formed through lateral epitaxial growth. Thereafter, the remaining GaN layer 31 is removed through etching, together with the GaN layer 32 formed atop the GaN layer 31, and subsequently, a GaN layer 33 is lateral-epitaxially grown with the top surfaces of mesas and sidewalls of trenches serving as nuclei, the mesas and trenches being formed of the remaining GaN layer 32, thereby producing a GaN substrate 30 in which threading dislocations are considerably suppressed. When the area of a portion of the GaN layer 31 at which the GaN substrate 30 is in contact with the substrate base 1 is reduced, separation of the GaN substrate 30 from the substrate base 1 is readily attained.

FIG. 1A

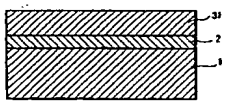


FIG. 1B

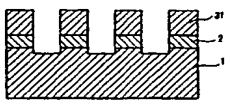


FIG. 1C

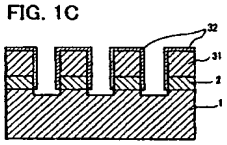
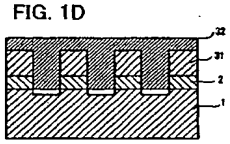


FIG. 1D



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Description

Technical Field

[0001] The present invention relates to a method for fabricating Group III nitride compound semiconductor substrates. More particularly, the present invention relates to a method for fabricating Group III nitride compound semiconductor substrates employing epitaxial lateral overgrowth (ELO). Like the case of semiconductor substrates produced by methods other than the method of the present invention, the Group III nitride compound semiconductor substrate produced by the method of the present invention is useful for forming a semiconductor device. The Group III nitride compound semiconductors are generally represented by $Al_xGa_yIn_{1-x-y}N$ (wherein $0 \leq x \leq 1$, $0 \leq y \leq 1$, and $0 \leq x + y \leq 1$), and examples thereof include binary semiconductors such as AlN, GaN, and InN; ternary semiconductors such as $Al_xGa_{1-x}N$, $Al_xIn_{1-x}N$, and $Ga_xIn_{1-x}N$ (wherein $0 < x < 1$); and quaternary semiconductors such as $Al_xGa_yIn_{1-x-y}N$ (wherein $0 < x < 1$, $0 < y < 1$, and $0 < x + y < 1$). In the present specification, unless otherwise specified, "Group III nitride compound semiconductors" comprise Group III nitride compound semiconductors which are doped with an impurity so as to get p-type or n-type conductivity.

Background Art

[0002] Group III nitride compound semiconductor are direct-transition type of semiconductors exhibiting a wide range of emission spectra from UV to red light when used in a device such as a light-emitting device, for example, light-emitting diodes (LEDs) and laser diodes (LDs). In addition, due to their wide band gaps, devices employing the aforementioned semiconductors are expected to exhibit reliable operational characteristics at high temperature as compared with those employing semiconductors of other types, and thus application thereof to transistors such as FETs has been energetically studied. Moreover, because Group III nitride compound semiconductors contain no arsenic (As) as a predominant element, application of Group III nitride compound semiconductors to various semiconductor elements has been expected from the environmental aspect. Generally, these Group III nitride compound semiconductors are formed on a sapphire substrate.

Disclosure of the Invention

[0003] However, when a Group III nitride compound semiconductor is formed on a sapphire substrate, misfit-induced dislocations occur due to difference between the lattice constant of sapphire and that of the semiconductor, resulting in poor device characteristics. Misfit-induced dislocations are threading dislocations which penetrate semiconductor layers in a longitudinal direction (i.e., in a direction vertical to the surface of the substrate), and Group III nitride compound semiconductors are accompanied by the problem that dislocations in amounts of approximately 10^9 cm^{-2} propagate therethrough. The aforementioned dislocations propagate through layers formed from Group III nitride compound semiconductors of different compositions, until they reach the uppermost layer. When such a semiconductor is incorporated in, for example, a light-emitting device, the device poses problems of unsatisfactory device characteristics in terms of threshold current of an LD, a life time of an LED or LD, etc. On the other hand, when a Group III nitride compound semiconductor is incorporated in any of other types of semiconductor devices, because electrons are scattered due to defects in the Group III nitride compound semiconductor, the semiconductor element comes to have low mobility. These problems are not solved even when another type of substrate is employed.

[0004] The aforementioned dislocations will next be described with reference to a schematic representation shown in FIG. 9. FIG. 9 shows a substrate 91, a buffer layer 92 formed thereon, and a Group III nitride compound semiconductor layer 93 further formed thereon. Conventionally, the substrate 91 is formed of sapphire or a similar substance and the buffer layer 92 is formed of aluminum nitride (AlN) or a similar substance. The buffer layer 92 formed of aluminum nitride (AlN) is provided so as to relax misfit between the sapphire substrate 91 and the Group III nitride compound semiconductor layer 93. However, generation of dislocations is not reduced to zero. Threading dislocations 901 propagate upward (in a vertical direction with respect to the substrate surface) from dislocation initiating points 900, penetrating the buffer layer 92 and the Group III nitride compound semiconductor layer 93. When a semiconductor device is fabricated by laminating various types of Group III nitride compound semiconductors of interest on the Group III nitride compound semiconductor layer 93, threading dislocations further propagate upward, through the semiconductor device, from dislocation arrival points 902 on the surface of the Group III nitride compound semiconductor layer 93. Thus, according to conventional techniques, problematic propagation of dislocations cannot be prevented during formation of Group III nitride compound semiconductor layers.

[0005] There have been proposed techniques in which a thick Group III nitride compound semiconductor layer is formed on a substrate base formed of a compound different from a Group III nitride compound, and subsequently the substrate base is removed, to thereby produce a Group III nitride compound semiconductor substrate. Such techniques include a technique called ELO or Pendeo ELO. However, the aforementioned techniques have not been put into practice, since difficulty is encountered in removing a Group III nitride compound semiconductor substrate from the substrate base.

[0006] The present invention has been accomplished in an attempt to solve the aforementioned problems, and an object of the present invention is to provide a convenient method for fabricating a Group III nitride compound semiconductor substrate with suppressed generation of threading dislocations. Another object of the present invention is to provide a semiconductor device including the Group III nitride compound semiconductor substrate with suppressed generation of threading dislocations.

[0007] In order to solve the aforementioned problems, the invention drawn to a first feature provides a method for fabricating a Group III nitride compound semiconductor substrate through epitaxial growth of a Group III nitride compound semiconductor layer on a substrate base, followed by removal of the substrate base, which method comprises a step of forming an underlying layer on a substrate base, the underlying layer comprising at least one Group III nitride compound semiconductor layer, and the uppermost layer of the underlying layer being a first Group III nitride compound semiconductor layer; a first trench/mesa formation step in which at least a portion of the underlying layer and at least a portion of the surface of the substrate base are removed through etching so as to form an island-like structure having, for example, a dot, stripe, or grid shape, thereby providing a trench/mesa structure including mesas formed on the underlying layer and trenches whose bottoms sink into the surface of the substrate base; a first lateral epitaxial growth step in which a second Group III nitride compound semiconductor layer is epitaxially grown, vertically and laterally, with top surfaces of the mesas and sidewalls of the trenches serving as nuclei for crystal growth, i.e., seeds for crystal growth, the mesas and trenches being formed by etching of the first Group III nitride compound semiconductor layer so as to form an island-like structure having, for example, a dot, stripe, or grid shape, thereby filling upper portions of the trenches and covering the mesas; a second trench/mesa formation step in which the entire underlying layer that has not undergone etching in the first trench/mesa formation step, excepting a portion of the underlying layer, is removed by etching, together with the second Group III nitride compound semiconductor layer formed on the underlying layer, and at least a portion of the surface of the substrate base, so as to provide a trench/mesa structure including mesas formed on the remaining second Group III nitride compound semiconductor layer and trenches whose bottoms sink into the surface of the substrate base; a second lateral epitaxial growth step in which a third Group III nitride compound semiconductor layer is epitaxially grown, vertically and laterally, with top surfaces of the mesas and sidewalls of the trenches serving as nuclei for crystal growth, i.e., seeds for crystal growth, the mesas and trenches being formed through etching of the second Group III nitride compound semiconductor layer, thereby filling upper portions of the trenches and covering the mesas; and a step of removing the substrate base and the underlying layer which has not been removed in the second trench/mesa formation step, to thereby produce a substrate comprising the second and third Group III nitride compound semiconductor layers. In the present specification, the term "underlying layer" is used to collectively comprise a Group III nitride compound semiconductor single layer and a multi-lamellar layer containing at least one Group III nitride compound semiconductor layer. The expression "island-like structure" conceptually refers to the pattern of the upper portions of the mesas formed through etching, and does not necessarily refer to regions separated from one another. Thus, the upper portions of the mesas may be continuously connected to one another over a considerably wide area, and such a structure may be obtained by forming the entirety of a wafer into stripes or grids. The sidewall/sidewalls of the trench refer not only to planes that are vertical to the substrate plane and the surface of a Group III nitride compound semiconductor layer, but also to oblique planes. The trench may have a V-shaped cross section; i.e., the trench may have no bottom surface. The expression "filling upper portions of the trench" does not necessarily refer to the case where the upper portions are completely filled so as to provide no space, and a space may be provided. Examples of such a space include a space generated through incomplete growth of a Group III nitride compound semiconductor layer as a result of insufficient feeding of a raw or source material to epitaxial growth fronts starting from the sidewalls of the trench; and a gap between the substrate plane and a Group III nitride compound semiconductor layer. Unless otherwise specified, these definitions are equally applied to the below-described features.

[0008] The invention drawn to a second feature provides a method for fabricating a Group III nitride compound semiconductor substrate comprising epitaxial growth of a Group III nitride compound semiconductor layer on a substrate base, and removal of the substrate base, which method comprises a step of forming an underlying layer on a substrate base, the underlying layer comprising at least one Group III nitride compound semiconductor layer, and the uppermost layer of the underlying layer being a first Group III nitride compound semiconductor layer; a first trench/mesa formation step in which the underlying layer is etched so as to form an island-like structure having, for example, a dot, stripe, or grid shape, thereby providing a trench/mesa structure, such that the substrate base is exposed so as to provide the bottoms of trenches; a first mask formation step in which first masks are formed at the bottoms of the trenches formed in the first trench/mesa formation step, such that the upper surfaces of the first masks are positioned below the top surface of the uppermost layer of the underlying layer; a first lateral epitaxial growth step in which a second Group III nitride compound semiconductor layer is epitaxially grown, vertically and laterally, with top surfaces of mesas and sidewalls of the

trenches serving as nuclei for crystal growth, i.e., seeds for crystal growth, the mesas and trenches being formed by etching of the first Group III nitride compound semiconductor layer so as to form an island-like structure having, for example, a dot, stripe, or grid shape, thereby filling spaces above the first masks and covering the mesas; a second trench/mesa formation step in which substantially the entire underlying layer that has not undergone etching in the first trench/mesa formation step is removed through etching, together with the second Group III nitride compound semiconductor layer formed on the underlying layer, so as to provide a trench/mesa structure including mesas formed on the remaining second Group III nitride compound semiconductor layer and trenches such that the substrate base is exposed so as to provide the bottoms of the trenches; a second mask formation step in which second masks are formed at the bottoms of the trenches formed in the second trench/mesa formation step, such that the upper surfaces of the second masks are positioned below the top surface of the second Group III nitride compound semiconductor layer; a second lateral epitaxial growth step in which a third Group III nitride compound semiconductor layer is epitaxially grown, vertically and laterally, with top surfaces of the mesas and sidewalls of the trenches serving as nuclei for crystal growth, i.e., seeds for crystal growth, the mesas and trenches being formed by etching of the second Group III nitride compound semiconductor layer, thereby filling spaces above the second masks and covering the mesas; a step of removing the first and second masks by wet etching; and a step of removing the substrate base, to thereby produce a substrate comprising the second and third Group III nitride compound semiconductor layers.

[0009] The invention drawn to a third feature provides a method for fabricating a Group III nitride compound semiconductor substrate as recited in connection with the second feature, wherein the masks are formed of a substance capable of impeding epitaxial growth of a Group III nitride compound semiconductor layer on the masks.

[0010] The invention drawn to a fourth feature provides a method for fabricating a Group III nitride compound semiconductor substrate as recited in connection with any one of the first through third features, wherein virtually all the sidewalls of the trenches formed in the first and second trench/mesa formation steps are a {11-20} plane.

[0011] The invention drawn to a fifth feature provides a method for fabricating a Group III nitride compound semiconductor substrate as recited in connection with any one of the first through fourth features, wherein the first Group III nitride compound semiconductor layer and the second Group III nitride compound semiconductor layer have the same composition. In the context of the present invention, compositions which differ from one another on doping level (differences of less than 1 mol%) are referred to as the "same composition."

[0012] The invention drawn to a sixth feature provides a method for fabricating a Group III nitride compound semiconductor substrate as recited in connection with any one of the first through fifth features, wherein the second Group III nitride compound semiconductor layer and the third Group III nitride compound semiconductor layer have the same composition. In the context of the present invention, compositions which differ from one another on doping level (differences of less than 1 mol%) are referred to as the "same composition."

[0013] The invention drawn to a seventh feature provides a Group III nitride compound semiconductor device, which is formed on a Group III nitride compound semiconductor substrate produced through a method for fabricating a Group III nitride compound semiconductor substrate as recited in connection with any one of the first through sixth features.

[0014] The invention drawn to an eighth feature provides a Group III nitride compound semiconductor light-emitting device, which is produced by laminating a different Group III nitride compound semiconductor layer on a Group III nitride compound semiconductor substrate produced through a method for fabricating a Group III nitride compound semiconductor substrate as recited in connection with any one of the first through sixth features.

[0015] The outline of the method for fabricating a Group III nitride compound semiconductor substrate of the present invention will next be described with reference to FIGs. 1 through 4. Although FIGs. 1 and 3 illustrate structures including a substrate base 1 and a buffer layer 2, the buffer layer 2 is not an essential element of the present invention, in view that the object of the present invention is to produce, by performing etching twice and lateral epitaxial growth twice, a Group III nitride compound semiconductor substrate having reduced threading dislocations in the vertical direction from a first Group III nitride compound semiconductor layer having threading dislocations in the vertical direction. The gist of the operation and effects of the present invention will next be described with reference to embodiments in which a first Group III nitride compound semiconductor layer 31 having threading dislocations in the vertical direction (direction vertical to the substrate surface) is formed above the substrate base 1 via the buffer layer 2.

[0016] As shown in FIG. 1(a), the first Group III nitride compound semiconductor layer 31 is formed above the substrate base 1 via the buffer layer 2. Subsequently, as shown in FIG. 1(b), the first Group III nitride compound semiconductor layer 31 is subjected to etching, so as to form an island-like structure having, for example, a dot, stripe, or grid shape, thereby providing first trenches/mesas such that depressions of the substrate base 1 are exposed so as to form the bottoms of the trenches. Subsequently, a second Group III nitride compound semiconductor layer 32 is epitaxially grown, vertically and laterally, with top surfaces of the first mesas

or posts and sidewalls of the first trenches serving as nuclei for crystal growth, i.e., seeds for crystal growth, to thereby fill spaces above the trenches of the substrate base 1, while epitaxial growth is effected in the vertical direction. In this case, propagation of threading dislocations contained in the first Group III nitride compound semiconductor layer 31 can be prevented in the upper portion of the second Group III nitride compound semiconductor layer 32 that is formed by lateral epitaxial growth (FIGs. 1(c) and 1(d)). That is, no threading dislocations propagate, in the vertical direction, through a portion that is laterally grown with the sidewalls of the trenches serving as nuclei for crystal growth. The first Group III nitride compound semiconductor layer 31 is strongly bonded to the substrate base 1 via the buffer layer 2. Meanwhile, the second Group III nitride compound semiconductor layer 32 is not strongly bonded to the substrate base 1, since the layer 32 is not in direct contact with the substrate base 1, or the area of a portion at which the layer 32 is in direct contact with the substrate base 1 is very small. Therefore, portions of the second Group III nitride compound semiconductor layer 32 that are formed above the trenches of the substrate base 1 do not receive stress directly from the substrate base 1.

[0017] Subsequently, the first mesas (i.e., the first Group III nitride compound semiconductor layer 31 and the buffer layer 2 that have not undergone etching) are subjected to etching, together with the second Group III nitride compound semiconductor layer 32 formed on the layer 31. The substrate base 1 is also subjected to etching, to thereby form depressions or trenches. This etching provides second trenches/mesas; i.e., laterally epitaxially grown portions of the second Group III nitride compound semiconductor layer 32 (FIG. 2(e)). When, although not illustrated in FIG. 2(e), the first Group III nitride compound semiconductor layer 31 is caused to partially remain on the substrate base and to be bonded thereto, the mesas formed of the second Group III nitride compound semiconductor layer 32 can be provided over a wide region as shown in FIG. 2(e), in which the mesas can be viewed as if they were floating above the substrate base. In this case, threading dislocations are considerably reduced in the second Group III nitride compound semiconductor layer 32 which has been formed as the second mesas. Subsequently, a third Group III nitride compound semiconductor layer 33 is epitaxially grown, vertically and laterally, with top surfaces of the second mesas and sidewalls of the second trenches serving as nuclei for crystal growth, i.e., seeds for crystal growth, which are formed of the second Group III nitride compound semiconductor layer 32 (FIG. 2(f)). The thus-grown third Group III nitride compound semiconductor layer 33 has virtually no threading dislocations that propagate therethrough in the vertical direction. Like the case of the second Group III nitride compound semiconductor layer 32, the third Group III nitride compound semiconductor layer 33 has virtually no contact with the substrate base 1. Therefore, portions of the third Group III nitride compound semiconductor layer 33 that are formed above the trenches of the substrate base 1 do not receive stress directly from the substrate base 1. After the third Group III nitride compound semiconductor layer 33 is formed so as to have a large thickness (FIG. 2(g)), the substrate base 1 is removed, to thereby produce a Group III nitride compound semiconductor substrate 30 having virtually no threading dislocations (FIG. 2(h)). The substrate base 1 is bonded to the Group III nitride compound semiconductor substrate 30 by means of merely a portion including the first Group III nitride compound semiconductor layer 31 and the buffer layer 2 that have remained during formation of the second trenches/mesas, and the area of the portion is very small. When the portion is removed together with the base substrate 1, or when the portion including the first Group III nitride compound semiconductor layer 31 and the buffer layer 2 is separated from the second and third Group III nitride compound semiconductor layers 32 and 33 formed above the trenches of the substrate base 1, the Group III nitride compound semiconductor substrate 30 having virtually no threading dislocations can be readily produced. The expression "removing all the underlying layer, excepting a portion thereof" does not exclude the case in which a portion containing threading dislocations is present to some extent, for the sake of convenience in manufacture. The method of the present invention encompasses a process in which etching and vertical and lateral epitaxial growth are performed three times or more, and virtually all the underlying layer is removed, to thereby produce a Group III nitride compound semiconductor substrate; a process in which a fourth Group III nitride compound semiconductor layer is formed while the third Group III nitride compound semiconductor layer 33 is formed so as to have a large thickness; and a process in which a different epitaxial technique is employed (the first feature).

[0018] In the aforementioned process, in order to reduce the area of a portion at which the second or third Group III nitride compound semiconductor layer is in contact with the substrate base 1, the substrate base 1 is subjected to etching to thereby form depressions. Meanwhile, the following process as shown in FIGs. 3 and 4 may be performed: the surface of a substrate base 1 is exposed; masks 41 and 42 are formed on the thus-exposed substrate base 1; and the masks are removed through wet etching at the final step (i.e., the step subsequent to the step shown in FIG. 4(g)), to thereby provide a space between a Group III nitride compound semiconductor substrate and the substrate base 1 (the second feature). When the masks are formed of a substance capable of impeding epitaxial growth of a Group III nitride compound semiconductor layer on the masks, during epitaxial growth and after epitaxial growth, the Group III nitride compound semiconductor layer does not receive stress from the substrate base 1 via the masks (the third feature).

[0019] The aforementioned rapid lateral epitaxial growth can be readily attained when the sidewalls of the trenches formed by etching of the Group III nitride compound semiconductor layer 31 are a {11-20} plane (the fourth feature). During lateral epitaxial growth, at least an upper portion of the growth front may remain a {11-20} plane. When the first Group III nitride compound semiconductor layer and the second Group III nitride compound semiconductor layer have the same composition, rapid lateral epitaxial growth can be readily attained (the fifth feature). Similar to the case described above, when the second Group III nitride compound semiconductor layer and the third Group III nitride compound semiconductor layer have the same composition, rapid lateral epitaxial growth can be readily attained (the sixth feature).

[0020] Through the procedure described above, the Group III nitride compound semiconductor substrate 30 can be readily removed from the substrate base 1, and threading dislocations contained in the substrate 30 can be reduced to the lowest possible level. Although FIGs. 1 through 4 illustrate sidewalls of trenches vertical to the substrate base, the present invention is not limited thereto, and the sidewalls may be oblique planes. So long as the first Group III nitride compound semiconductor layer 31 and the buffer layer 2 are removed through a combination of the first and second trench/mesa formation steps, the trenches formed in the first or second trench/mesa formation step may have V-shaped cross sections. These features are equally applied to the descriptions below.

[0021] When a device is formed on the Group III nitride compound semiconductor substrate produced through the above process, a semiconductor device having a layer containing few defects and endowed with high mobility can be provided (the seventh feature).

[0022] When a light-emitting device is formed on the Group III nitride compound semiconductor substrate produced through the above process, a light-emitting device endowed with improved life time and an improved LD threshold value can be provided (the eighth feature).

Brief Description of the Drawings

[0023]

FIG. 1 is a series of cross-sectional views showing the first half of the steps of fabricating a Group III nitride compound semiconductor substrate according to a first embodiment of the present invention.

FIG. 2 is a series of cross-sectional views showing the second half of the steps of fabricating a Group III nitride compound semiconductor substrate according to the first embodiment of the present invention.

FIG. 3 is a series of cross-sectional views showing the first half of the steps of fabricating a Group III nitride compound semiconductor substrate according to a second embodiment of the present invention.

FIG. 4 is a series of cross-sectional views showing the second half of the steps of fabricating a Group III nitride compound semiconductor substrate according to the second embodiment of the present invention.

FIG. 5 is a schematic representation showing an example of etching of first and second Group III nitride compound semiconductor layers, and the second and third Group III nitride compound semiconductor layers which have been formed.

FIG. 6 is a cross-sectional view showing the structure of a Group III nitride compound semiconductor light-emitting device according to a third embodiment of the present invention.

FIG. 7 is a cross-sectional view showing the structure of a Group III nitride compound semiconductor light-emitting device according to a fourth embodiment of the present invention.

FIG. 8 is a schematic representation showing another example of etching of the first Group III nitride compound semiconductor layer.

FIG. 9 is a cross-sectional view showing threading dislocations propagating in a Group III nitride compound semiconductor.

Best Mode for Carrying Out the Invention

[0024] FIGs. 1 through 4 schematically show a mode for carrying out the method for fabricating a Group III nitride compound semiconductor substrate of the present invention. A substrate base 1, a buffer layer 2, and a first Group III nitride compound semiconductor layer 31 are formed (FIG. 1(a)), and the layers 2 and 31 are subjected to etching, to thereby form trenches (FIG. 1(b)). As a result of etching, first mesas and trenches are formed, the unetched surfaces of the layer 31 become the top surfaces of the mesas, sidewalls of the trenches are formed, and bottoms of the trenches are formed; i.e., depressions are formed on the substrate base 1. The sidewalls are, for example, {11-20} planes. Subsequently, under conditions of lateral epitaxial growth, a second Group III nitride compound semiconductor layer 32 is epitaxially grown with the sidewalls of the first trenches and the top surfaces of the first mesas serving as nuclei for crystal growth, i.e., seeds for crystal growth. A metal-organic growth process enables easy lateral epitaxial growth while the growth fronts remain the {11-20} planes. Portions of the second Group III nitride compound semiconductor layer 32 that are laterally grown from the sidewalls of the trenches are free from propagation of threading dislocations (FIG. 1(c)). The form of etching and lateral epitaxial growth conditions are determined such that the fronts of lateral growth extending from the opposite sidewalls of the trenches fill the etched trenches, whereby threading dislocations are

suppressed in the regions of the second Group III nitride compound semiconductor layer 32 formed above the bottoms of the etched trenches (FIG. 1(d)). Thereafter, the first Group III nitride compound semiconductor layer 31 and the buffer layer 2 are removed by etching, together with the second Group III nitride compound semiconductor layer 32 formed on the layer 31, and the surface of the substrate base 1, to thereby provide second trenches/mesas formed of the second Group III nitride compound semiconductor layer 32 with suppressed threading dislocations (FIG. 2(e)). When, although not illustrated in FIG. 2(e), the first Group III nitride compound semiconductor layer 31 is caused to partially remain on the substrate base and to be bonded thereto, the mesas formed of the second Group III nitride compound semiconductor layer 32 can be provided over a wide region as shown in FIG. 2(e), in which the mesas can be viewed as if they were floating above the substrate base. Subsequently, a third Group III nitride compound semiconductor layer 33 is epitaxially grown, vertically and laterally, with top surfaces of the second mesas and sidewalls of the second trenches serving as nuclei for crystal growth, i.e., seeds for crystal growth, the mesas and trenches being formed of the second Group III nitride compound semiconductor layer 32 with suppressed threading dislocations (FIG. 2(f)), whereby virtually no threading dislocations are generated in the third Group III nitride compound semiconductor layer 33. After the third Group III nitride compound semiconductor layer 33 is formed so as to have a large thickness (FIG. 2(g)), the substrate base 1 is removed, to thereby produce a Group III nitride compound semiconductor substrate 30 (FIG. 2(h)). The substrate base 1 is bonded to the Group III nitride compound semiconductor substrate 30 via merely a portion including the first Group III nitride compound semiconductor layer 31 and the buffer layer 2 that have remained during formation of the second trenches/mesas. Therefore, when the portion is removed, or when the portion is separated from the second and third Group III nitride compound semiconductor layers 32 and 33, the Group III nitride compound semiconductor substrate 30 is produced. As shown in FIGs. 3 and 4, when masks 41 on which a Group III nitride compound semiconductor layer is not epitaxially grown are provided at the bottoms of the first trenches, and masks 42 on which a Group III nitride compound semiconductor layer is not epitaxially grown are provided at the bottoms of the second trenches, in a manner similar to that described above, the Group III nitride compound semiconductor substrate 30 can be readily produced. The masks 41 and 42 are preferably formed of a substance which can be removed through, for example, wet etching.

[0025] There may be employed an underlying layer including a plurality of sub-layer units, each unit having a buffer layer and a Group III nitride compound semiconductor layer grown epitaxially on the buffer layer, wherein the lowermost unit includes a buffer layer formed directly on the substrate base 1. Regardless of the number of the units, the substrate base 1 is exposed through the bottoms of the trenches formed in the underlying layer. Portions of the Group III nitride compound semiconductor layer 32 formed above the bottoms of the trenches are formed primarily through lateral epitaxial growth while the Group III nitride compound semiconductor layer 31, which is the top layer of the mesas, serves as nuclei, thereby becoming regions in which threading dislocations of vertical propagation are suppressed.

[0026] The aforementioned modes for carrying out the invention may employ any of the following processes.

[0027] When Group III nitride compound semiconductor layers are successively formed on a substrate base, the substrate base may be formed from an inorganic crystal compound such as sapphire, silicon (Si), silicon carbide (SiC), spinel ($MgAl_2O_4$), ZnO, or MgO; a Group III-V compound semiconductor such as gallium phosphide or gallium arsenide; or a Group III nitride compound semiconductor having threading dislocations, such as gallium nitride (GaN).

[0028] A preferred process for forming a Group III nitride compound semiconductor layer is metal-organic chemical vapor deposition (MOCVD) or metal-organic vapor phase epitaxy (MOVPE). However, molecular beam epitaxy (MBE), halide vapor phase epitaxy (Halide VPE), liquid phase epitaxy (LPE), or the like may be used. Also, individual layers may be formed by different growth processes.

[0029] When a Group III nitride compound semiconductor layer is to be formed on, for example, a sapphire substrate serving as a substrate base, in order to impart good crystallinity to the layer, a buffer layer is preferably formed for the purpose of correcting lattice mismatch with the sapphire substrate. When a substrate of another material is to be used as a substrate base, employment of a buffer layer is also preferred. A buffer layer is preferably of a Group III nitride compound semiconductor $Al_xGa_yIn_{1-x-y}N$ formed at low temperature ($0 \leq x \leq 1$, $0 \leq y \leq 1$, $0 \leq x + y \leq 1$), more preferably of $Al_xGa_{1-x}N$ ($0 \leq x \leq 1$). This buffer layer may be a single layer or a multicomponent layer containing layers of different compositions. A buffer layer may be formed at a low temperature of 380 to 420°C or by MOCVD at a temperature of 1,000 to 1,180°C. Alternatively, an AlN buffer layer can be formed by a reactive sputtering process using a DC magnetron sputtering apparatus and, as materials, high-purity aluminum and nitrogen gas. Similarly, a buffer layer represented by the formula $Al_xGa_yIn_{1-x-y}N$ ($0 \leq x \leq 1$, $0 \leq y \leq 1$, $0 \leq x + y \leq 1$, arbitrary composition) can be formed. Furthermore, vapor deposition, ion plating, laser abrasion, or ECR can be employed. When a buffer layer is to be formed by physical vapor deposition, physical vapor deposition is performed preferably at 200 to 600°C, more preferably 300 to 500°C, most preferably 350 to 450°C. When physical vapor deposition, such as

sputtering, is employed, the thickness of a buffer layer is preferably 100 to 3,000 Å, more preferably 100 to 400 Å, most preferably 100 to 300 Å. A multi-component layer may contain, for example, alternating $Al_xGa_{1-x}N$ ($0 \leq x \leq 1$) layers and GaN layers. Alternatively, a multi-component layer may contain alternating layers of the same composition formed at a temperature of not higher than 600°C and at a temperature of not lower than 1,000°C. Of course, these arrangements may be combined. Also, a multi-component layer may contain three or more different types of Group III nitride compound semiconductors $Al_xGa_yIn_{1-x-y}N$ ($0 \leq x \leq 1$, $0 \leq y \leq 1$, $0 \leq x + y \leq 1$). Generally, a buffer layer is amorphous and an intermediate layer is monocrystalline. Repetitions of unit of a buffer layer and an intermediate layer may be formed, and the number of repetitions is not particularly limited. The greater the number of repetitions, the greater the improvement in crystallinity.

[0030] The present invention is substantially applicable even when the composition of a buffer layer and that of a Group III nitride compound semiconductor formed on the buffer layer are such that a portion of Group III elements are replaced with boron (B) or thallium (Tl) or a portion of nitrogen (N) atoms are replaced with phosphorus (P), arsenic (As), antimony (Sb), or bismuth (Bi). Also, the buffer layer and the Group III nitride compound semiconductor may be doped with any one of these elements to such an extent as not to appear in the composition thereof. For example, a Group III nitride compound semiconductor which is represented by $Al_xGa_{1-x}N$ ($0 \leq x \leq 1$) and which does not contain indium (In) and arsenic (As) may be doped with indium (In), which is larger in atomic radius than aluminum (Al) and gallium (Ga), or arsenic (As), which is larger in atomic radius than nitrogen (N), to thereby improve crystallinity through compensation, by means of compression strain, for crystalline expansion strain induced by dropping off of nitrogen atoms. In this case, since acceptor impurities easily occupy the positions of Group III atoms, p-type crystals can be obtained as grown. Through the thus-attained improvement of crystallinity combined with the features of the present invention, threading dislocation can be further reduced to approximately 1/100 to 1/1,000. In the case of an underlying layer containing two or more repetitions of a buffer layer and a Group III nitride compound semiconductor layer, the Group III nitride compound semiconductor layers are further preferably doped with an element greater in atomic radius than a predominant component element. When a light-emitting element is produced after formation of a Group III nitride compound semiconductor substrate, use of a binary or ternary Group III nitride compound semiconductor is preferred.

[0031] When an n-type Group III nitride compound semiconductor layer is to be formed, a Group IV or Group VI element, such as Si, Ge, Se, Te, or C, can be added as an n-type impurity. A Group II or Group IV element, such as Zn, Mg, Be, Ca, Sr, or Ba, can be added as a p-type impurity. The same layer may be doped with a plurality of n-type or p-type impurities or doped with both n-type and p-type impurities. Thus, an n-type or p-type Group III nitride compound semiconductor substrate having arbitrary conductivity can be produced.

[0032] Lateral epitaxial growth preferably progresses such that the front of lateral epitaxial growth is perpendicular to a substrate base. However, lateral epitaxial growth may progress while slant facets with respect to the substrate base are maintained. In this case, trenches may have a V-shaped cross section.

[0033] Preferably, lateral epitaxial growth progresses such that at least an upper portion of the front of lateral epitaxial growth is perpendicular to the surface of a substrate base. More preferably, growth fronts are {11-20} planes of a Group III nitride compound semiconductor layer.

[0034] The depth and width of trenches to be etched are appropriately determined such that lateral epitaxial growth fills the trenches.

[0035] When the crystal orientation of a Group III nitride compound semiconductor layer to be formed on a substrate base can be predicted, masking or etching in the form of stripes perpendicular to the a-plane ({11-20} plane) or the m-plane ({1-100} plane) of the Group III nitride compound semiconductor layer is favorable. The aforementioned stripe or mask patterns may be island-like or grid-like or may assume other forms. The front of lateral epitaxial growth may be perpendicular or oblique to the surface of a substrate base. In order for the a-plane; i.e., the (11-20) plane, of a Group III nitride compound semiconductor layer to become the front of lateral epitaxial growth, the lateral direction of stripes must, for example, be perpendicular to the m-plane; i.e., the (1-100) plane, of the Group III nitride compound semiconductor layer. For example, when the surface of a substrate base is the a-plane or the c-plane of sapphire, the m-plane of sapphire usually matches the a-plane of a Group III nitride compound semiconductor layer formed on the substrate base. Thus, etching is performed according to the arrangement of the planes. In the case of dot-like, grid-like, or island-like etching, planes that define an outline (sidewalls) are preferably {11-20} planes.

[0036] An etching mask may be formed of a multi-layer film formed from a polycrystalline semiconductor such as polycrystalline silicon or a polycrystalline nitride semiconductor; an oxide or a nitride, such as silicon oxide (SiO_x), silicon nitride (SiN_x), titanium oxide (TiO_x), or zirconium oxide (ZrO_x); or a metal of high melting point, such as titanium (Ti) or tungsten (W). The film may be formed through any known method, such as a vapor-growth method (e.g., deposition, sputtering, or CVD). The mask may be removed during lateral epitaxial growth, or a Group III nitride compound semiconductor layer may be laterally epitaxially grown so as to cover the mask without removal of the mask. When the mask is removed, the laterally epitaxially grown Group III ni-

tride compound semiconductor layer exhibits improved crystallinity. Meanwhile, when the mask is caused to remain, dislocations may be generated at the edge of the mask.

[0037] Reactive ion etching (RIE) is preferred, but any other etching process may be employed. When trenches having sidewalls oblique to the surface of a substrate base are to be formed, anisotropic etching is employed. By means of anisotropic etching, trenches are formed such that the trenches have a V-shaped cross section.

[0038] No particular limitation is imposed on the mask provided at the bottoms of trenches, so long as the mask can be removed through wet etching. Therefore, the aforementioned etching mask may be employed. The mask provided at the bottoms of the trenches may be removed through any wet etching technique. When the mask provided at the bottoms of the trenches is formed of silicon dioxide, the mask may be removed through wet etching employing a hydrofluoric-acid-based etchant.

[0039] A semiconductor device, such as an FET or a light-emitting device, can be formed on the aforementioned Group III nitride compound semiconductor substrate having virtually no threading dislocations. In the case where a light-emitting device is formed, a light-emitting layer may have a multi-quantum well (MQW) structure, a single-quantum well (SQW) structure, a homo-structure, a single-hetero-structure, or a double-hetero-structure, or the layer may be formed by means of, for example, a pin junction or a pn junction.

[0040] In order to separate the aforementioned Group III nitride compound semiconductor substrate having virtually no threading dislocations from the substrate base 1, any known technique, such as mechanochemical polishing, may be employed. The Group III nitride compound semiconductor substrate produced through the method of the present invention may be employed for forming a larger Group III nitride compound semiconductor crystal.

[0041] Embodiments of the present invention in which light-emitting elements are produced will next be described. The present invention is not limited to the embodiments described below. The present invention discloses a method for fabricating a Group III nitride compound semiconductor substrate applicable to fabrication of any device.

[0042] The Group III nitride compound semiconductor of the present invention was produced through metal-organic vapor phase epitaxy (hereinafter called "MOVPE"). The following gasses were employed: ammonia (NH_3), carrier gas (H_2 or N_2), trimethylgallium ($Ga(CH_3)_3$, hereinafter called "TMG"), trimethylaluminum ($Al(CH_3)_3$, hereinafter called "TMA"), trimethylindium ($In(CH_3)_3$, hereinafter called "TMI"), and cyclopentadienylmagnesium ($Mg(C_5H_5)_2$, hereinafter called "Cp_2Mg").

[First embodiment]

[0043] FIGs. 1 and 2 show the steps of the present embodiment. A monocrystalline sapphire substrate 1 whose principle surface for crystal growth is an a-plane was cleaned by organic cleaning and heat treatment. The temperature of the substrate 1 was lowered to 400°C, and H_2 (10 L/min), NH_3 (5 L/min), and TMA (20 μmol/min) were fed for about three minutes, to thereby form an AlN buffer layer 2 (thickness: about 40 nm) on the substrate 1. Subsequently, while the temperature of the sapphire substrate 1 was maintained at 1,000°C, H_2 (20 L/min), NH_3 (10 L/min), and TMG (300 μmol/min) were introduced, to thereby form a GaN layer 31 (thickness: about 1 μm) (FIG. 1(a)).

[0044] By use of a hard bake resist mask, stripe-shaped trenches each having a width of 10 μm and a depth of about 1.2 μm were formed at intervals of 10 μm through selective dry etching employing reactive ion etching (RIE). As a result, mesas formed of the GaN layer 31 and the buffer layer 2 each having a width of 10 μm and a height of about 1 μm, and depressions of the sapphire substrate 1 each having a depth of 0.2 μm were alternately formed (FIG. 1(b)). At this time, the {11-20} planes of the GaN layer 31 were caused to serve as the sidewalls of the trenches of a depth of 1 μm.

[0045] Subsequently, while the temperature of the sapphire substrate 1 was maintained at 1,150°C, H_2 (20 L/min), NH_3 (10 L/min), and TMG (2 μmol/min) were introduced, to thereby form a GaN layer 32 by lateral epitaxial growth performed while the sidewalls of the trenches of a depth of 1 μm; i.e., the {11-20} planes of the GaN layer 31, served as nuclei for crystal growth. At an initial stage, vertical epitaxial growth from the top surfaces of the mesas or posts was suppressed (FIG. 1(c)). Lateral epitaxial growth was performed while the {11-20} planes primarily served as the growth fronts, whereby the trenches were filled, and the surface of the GaN layer 32 became flat. The overall thickness of the GaN layer 31 and the GaN layer 32 was found to be about 1.5 μm (FIG. 1(d)).

[0046] Subsequently, by use of a hard bake resist mask, stripe-shaped trenches each having a width of 10 μm and a depth of about 1.7 μm were formed at intervals of 10 μm through selective dry etching employing reactive ion etching (RIE), whereby virtually all the GaN layer 31 and the buffer layer 2 was removed, together with the GaN layer 32 formed atop the GaN layer 31 and the surface of the sapphire substrate 1 (FIG. 2(e)). FIG. 5 schematically shows the thus-formed structure. Specifically, FIG. 5(a) is a plan view corresponding to FIG. 1 (b), and reference letter B of FIG. 5(a) denotes the depressions or trenches formed in the sapphire substrate 1. FIG. 5(b) is a plan view corresponding to FIG. 2(e), and reference letter A of FIG. 5(b) denotes the exposed depressions or trenches of the sapphire substrate 1. As shown in FIG. 5(b) (not illustrated in FIG. 2(e)), the GaN layer 31 is caused to remain on the periphery of the sap-

phire substrate 1.

[0047] Through the aforementioned etching, mesas formed of the GaN layer 32 each having a width of 10 μm and a height of about 1.5 μm, and trenches of the sapphire substrate 1 each having a width of 10 μm and a depth of 0.2 μm were alternately formed (FIG. 2(e)). At this time, the {11-20} planes of the GaN layer 32 were served as the sidewalls of the trenches of a depth of 1.5 μm.

[0048] Subsequently, while the temperature of the sapphire substrate 1 was maintained at 1,150°C, H_2 (20 L/min), NH_3 (10 L/min), and TMG (2 μmol/min) were introduced, to thereby form a GaN layer 33 through lateral epitaxial growth performed while the sidewalls of the trenches of a depth of 1.5 μm; i.e., the {11-20} planes of the GaN layer 32, served as nuclei for crystal growth. At an initial stage, vertical epitaxial growth from the top surfaces of the mesas was suppressed (FIG. 2(f)). Lateral epitaxial growth was performed while the {11-20} planes primarily served as the growth fronts, whereby the trenches were filled, and the surface of the GaN layer 33 became flat. Thereafter, H_2 (20 L/min), NH_3 (10 L/min), and TMG (300 μmol/min) were introduced, to thereby further grow the GaN layer 33 until the overall thickness of the GaN layer 32 and the GaN layer 33 became 300 μm (FIG. 2(g)). Thereafter, a GaN substrate 30 including the GaN layer 32 and the GaN layer 33 was separated, through dicing, from the sapphire substrate 1 and the remaining portion of the GaN layer 31 (see FIG. 5(c)) at the boundary between the GaN substrate 30 and the remaining portion of the GaN layer 31 (FIG. 2(h)). The thus-produced GaN substrate 30 was found to contain virtually no threading dislocations.

[Second embodiment]

[0049] FIGs. 3 and 4 show the steps of the present embodiment. A monocrystalline sapphire substrate 1 whose principal surface an a-plane was cleaned through organic cleaning and heat treatment. The temperature of the substrate 1 was lowered to 400°C, and H_2 (10 L/min), NH_3 (5 L/min), and TMA (20 μmol/min) were fed for about three minutes, to thereby form an AlN buffer layer 2 (thickness: about 40 nm) on the substrate 1. Subsequently, while the temperature of the sapphire substrate 1 was maintained at 1,000°C, H_2 (20 L/min), NH_3 (10 L/min), and TMG (300 μmol/min) were introduced, to thereby form a GaN layer 31 (thickness: about 1 μm).

[0050] By use of a hard bake resist mask, stripe-shaped trenches each having a width of 10 μm and a depth of about 1 μm were formed at intervals of 10 μm through selective dry etching employing reactive ion etching (RIE). As a result, mesas formed of the GaN layer 31 and the buffer layer 2 each having a width of 10 μm and a height of about 1 μm, and trenches each having a width of 10 μm and having the sapphire substrate 1 exposed at the bottom thereof were alternately formed (FIG. 3(a)). At this time, the {11-20} planes of the GaN layer 31 were served as the sidewalls of the trenches of a depth of 1 μm.

[0051] Subsequently, a silicon dioxide (SiO_2) film was uniformly formed through sputtering. Thereafter, a resist was applied onto the SiO_2 film; a portion of the resist that covered a necessary portion of the silicon dioxide film was remained through photolithography; and a portion of the silicon dioxide film that was not covered with the resist was subjected to wet etching, to thereby form a wafer having the structure shown in FIG. 3(b) and including masks 41.

[0052] Subsequently, while the temperature of the sapphire substrate 1 was maintained at 1,150°C, H_2 (20 L/min), NH_3 (10 L/min), and TMG (2 μmol/min) were introduced, to thereby form a GaN layer 32 through lateral epitaxial growth performed while the sidewalls of the trenches of a depth of 1 μm; i.e., the {11-20} planes of the GaN layer 31, served as nuclei for crystal growth. At an initial stage, vertical epitaxial growth from the top surfaces of the mesas was suppressed (FIG. 3(c)). Lateral epitaxial growth was performed while the {11-20} planes primarily served as the growth fronts, whereby the trenches were filled, and the surface of the GaN layer 32 became flat. The overall thickness of the GaN layer 31 and the GaN layer 32 was found to be about 1.5 μm (FIG. 3(d)).

[0053] Subsequently, by use of a hard bake resist mask, stripe-shaped trenches each having a width of 10 μm and a depth of about 1.5 μm were formed at intervals of 10 μm through selective dry etching employing reactive ion etching (RIE), whereby virtually the entirety of the GaN layer 31 and the buffer layer 2 were removed, together with the GaN layer 32 formed on the GaN layer 31. As a result, mesas formed of the GaN layer 32 each having a width of 10 μm and a height of about 1.5 μm, and trenches each having a width of 10 μm and having the sapphire substrate 1 exposed at the bottom thereof were alternately formed. At this time, the {11-20} planes of the GaN layer 32 were served as the sidewalls of the trenches of a depth of 1.5 μm. Subsequently, a silicon dioxide (SiO_2) film was uniformly formed through sputtering. Thereafter, a resist was applied onto the SiO_2 film; a portion of the resist that covered a necessary portion of the silicon dioxide film was caused to remain through photolithography; and a portion of the silicon dioxide film that was not covered with the resist was subjected to wet etching, to thereby form a wafer including SiO_2 masks 42 (FIG. 4(e)). The aforementioned procedure of the second embodiment is similar to that of the first embodiment, and the thus-formed structure is schematically shown in FIG. 5. Specifically, FIG. 5(a) is a plan view corresponding to FIG. 3(b), and reference letter B of FIG. 5(a) denotes the SiO_2 masks 41 formed on the sapphire substrate 1. FIG. 5(b) is a plan view corresponding to FIG. 4(e), and reference letter A of FIG. 5 (b) denotes the exposed SiO_2 masks 42 formed on the sapphire substrate 1. As shown in FIG. 5(b) (not illus-

trated in FIG. 4(e)), in consideration of workability, the GaN layer 31 is caused to remain on the periphery of the sapphire substrate 1.

[0054] Subsequently, while the temperature of the sapphire substrate 1 was maintained at 1,150°C, H_2 (20 L/min), NH_3 (10 L/min), and TMG (2 μmol/min) were introduced, to thereby form a GaN layer 33 through lateral epitaxial growth performed while the sidewalls of the trenches of a depth of 1.5 μm; i.e., the {11-20} planes of the GaN layer 32, served as nuclei for crystal growth. At an initial stage, vertical epitaxial growth from the top surfaces of the mesas was suppressed (FIG. 4(f)). Lateral epitaxial growth was performed while the {11-20} planes primarily served as the growth fronts, whereby the trenches were filled, and the surface of the GaN layer 33 became flat. Thereafter, H_2 (20 L/min), NH_3 (10 L/min), and TMG (300 μmol/min) were introduced, to thereby further grow the GaN layer 33 until the overall thickness of the GaN layer 32 and the GaN layer 33 became 300 μm (FIG. 4(g)). Subsequently, the SiO_2 masks 41 and 42 were removed through wet etching employing a hydrofluoric-acid-based etchant. Thereafter, a GaN substrate 30 including the GaN layer 32 and the GaN layer 33 was separated, through dicing, from the sapphire substrate 1 and the remaining portion of the GaN layer 31 (see FIG. 5(c)) at the boundary between the GaN substrate 30 and the remaining portion of the GaN layer 31 (FIG. 4(h)). The thus-produced GaN substrate 30 was found to contain virtually no threading dislocations.

[Third embodiment]

[0055] In the present embodiment, the first embodiment was modified such that silane (SiH_4) was fed during formation of the GaN layers 32 and 33, to thereby produce an n-type GaN substrate 101, and the thus-produced substrate 101 was employed. On the n-type GaN substrate 101, a silicon (Si)-doped n-$Al_{0.15}Ga_{0.85}N$ layer 102 (thickness: 2 μm) was formed at a temperature of 1,150°C through feeding of H_2 (10 L/min), NH_3 (10 L/min), TMG (100 μmol/min), TMA (10 μmol/min), and silane (SiH_4) diluted with H_2 gas to 0.86 ppm (0.2 μmol/min). On the n-$Al_{0.15}Ga_{0.85}N$ layer 102, a silicon (Si)-doped GaN n-guide layer 103, an MQW-structured light-emitting layer 104, a magnesium (Mg)-doped GaN p-guide layer 105, a magnesium (Mg)-doped $Al_{0.08}Ga_{0.92}N$ p-cladding layer 106, and a magnesium (Mg)-doped GaN p-contact layer 107 were formed. Subsequently, an electrode 108A of gold (Au) was formed on the p-contact layer 107, and an electrode 108B of aluminum (Al) was formed on the back side of the n-type GaN substrate 101 (FIG. 6). A laser diode (LD) 100 was formed on the n-type GaN substrate 101 containing virtually no threading dislocations. The thus-formed laser diode (LD) 100 exhibited significant improvement of life time and light-emitting efficiency.

[Fourth embodiment]

[0056] In the present embodiment, an n-type GaN substrate was employed. On an n-type GaN substrate 201, an n-$Al_{0.15}Ga_{0.85}N$ layer 202, a light-emitting layer 203, and a magnesium (Mg)-doped $Al_{0.15}Ga_{0.85}N$ p-cladding layer 204 were formed. Subsequently, an electrode 205A of gold (Au) was formed on the p-cladding layer 204, and an electrode 205B of aluminum (Al) was formed on the back side of the GaN substrate 201 (FIG. 7). The thus-formed light-emitting diode (LED) 200 exhibited significant improvement of life time and light-emitting efficiency.

[Modification of etching]

[0057] FIG. 8 shows an example in which island-like mesas are formed by means of three groups of {11-20} planes. To facilitate understanding, the schematic view of FIG. 8(a) includes a peripheral region formed by means of three groups of {11-20} planes. In actuality, tens of millions of island-like mesas may be formed per wafer. In FIG. 8(a), the area of the bottoms of the trenches B is three times the area of the top surfaces of the island-like mesas. In FIG. 8(b), the area of the bottoms of the trenches B is eight times the area of the top surfaces of the island-like mesas.

Claims

1. A method for fabricating a Group III nitride compound semiconductor substrate through epitaxial growth of a Group III nitride compound semiconductor layer on a substrate base, and removal of the substrate base, which method comprises a step of forming an underlying layer on a substrate base, the underlying layer comprising at least one Group III nitride compound semiconductor layer, and the uppermost layer of the underlying layer being a first Group III nitride compound semiconductor layer; a first trench/mesa formation step in which at least a portion of the underlying layer and at least a portion of the surface of the substrate base are removed through etching so as to form an island-like structure having, for example, a dot, stripe, or grid shape, thereby providing a trench/mesa structure including mesas formed on the underlying layer and trenches whose bottoms sink into the surface of the substrate base; a first lateral epitaxial growth step in which a second Group III nitride compound semiconductor layer is epitaxially grown, vertically and laterally, with top surfaces of the mesas and sidewalls of the trenches serving as nuclei for crystal growth, the mesas and trenches being formed by etching of the first Group III nitride compound semiconductor layer so as to form an island-like structure having, for example, a dot, stripe, or grid shape, thereby filling

upper portions of the trenches and covering the mesas; a second trench/mesa formation step in which the entire underlying layer that has not undergone etching in the first trench/mesa formation step, excepting a portion of the underlying layer, is removed by etching, together with the second Group III nitride compound semiconductor layer formed on the underlying layer, and at least a portion of the surface of the substrate base, so as to provide a trench/mesa structure including mesas formed on the remaining second Group III nitride compound semiconductor layer and trenches whose bottoms sink into the surface of the substrate base; a second lateral epitaxial growth step in which a third Group III nitride compound semiconductor layer is epitaxially grown, vertically and laterally, with top surfaces of the mesas and sidewalls of the trenches serving as nuclei for crystal growth, the mesas and trenches being formed through etching of the second Group III nitride compound semiconductor layer, thereby filling upper portions of the trenches and covering the mesas; and a step of removing the substrate base and the underlying layer which has not been removed in the second trench/mesa formation step, to thereby produce a substrate comprising the second and third Group III nitride compound semiconductor layers.

2. A method for fabricating a Group III nitride compound semiconductor substrate comprising epitaxial growth of a Group III nitride compound semiconductor layer on a substrate base, and removal of the substrate base, which method comprises a step of forming an underlying layer on a substrate base, the underlying layer comprising at least one Group III nitride compound semiconductor layer, and the uppermost layer of the underlying layer being a first Group III nitride compound semiconductor layer; a first trench/mesa formation step in which the underlying layer is etched so as to form an island-like structure having, for example, a dot, stripe, or grid shape, thereby providing a trench/mesa structure, such that the substrate base is exposed so as to provide the bottoms of trenches; a first mask formation step in which first masks are formed at the bottoms of the trenches formed in the first trench/mesa formation step, such that the upper surfaces of the first masks are positioned below the top surface of the uppermost layer of the underlying layer; a first lateral epitaxial growth step in which a second Group III nitride compound semiconductor layer is epitaxially grown, vertically and laterally, with top surfaces of mesas and sidewalls of the trenches serving as nuclei for crystal growth, the mesas and trenches being formed by etching of the first Group III nitride compound semiconductor layer so as to form an island-like structure having, for example, a dot, stripe, or grid shape, thereby filling spaces above the first masks and covering the mesas; a second trench/mesa formation step in which substantially the entire underlying layer that has not undergone etching in the first trench/mesa formation step is removed by etching, together with the second Group III nitride compound semiconductor layer formed on the underlying layer, so as to provide a trench/mesa structure including mesas formed on the remaining second Group III nitride compound semiconductor layer and trenches such that the substrate base is exposed so as to provide the bottoms of the trenches; a second mask formation step in which second masks are formed at the bottoms of the trenches formed in the second trench/mesa formation step, such that the upper surfaces of the second masks are positioned below the top surface of the second Group III nitride compound semiconductor layer; a second lateral epitaxial growth step in which a third Group III nitride compound semiconductor layer is epitaxially grown, vertically and laterally, with top surfaces of the mesas and sidewalls of the trenches serving as nuclei for crystal growth, the mesas and trenches being formed by etching of the second Group III nitride compound semiconductor layer, thereby filling spaces above the second masks and covering the mesas; a step of removing the first and second masks by wet etching; and a step of removing the substrate base, to thereby produce a substrate comprising the second and third Group III nitride compound semiconductor layers.

3. A method for fabricating a Group III nitride compound semiconductor substrate according to claim 2, wherein the masks are formed of a substance capable of impeding epitaxial growth of a Group III nitride compound semiconductor layer on the masks.

4. A method for fabricating a Group III nitride compound semiconductor substrate according to any one of claims 1 through 3, wherein virtually all the sidewalls of the trenches formed in the first and second trench/mesa formation steps are a {11-20} plane.

5. A method for fabricating a Group III nitride compound semiconductor substrate according to any one of claims 1 through 4, wherein the first Group III nitride compound semiconductor layer and the second Group III nitride compound semiconductor layer have the same composition.

6. A method for fabricating a Group III nitride compound semiconductor substrate according to any one of claims 1 through 5, wherein the second Group III nitride compound semiconductor layer and the third Group III nitride compound semiconductor layer have the same composition.

7. A Group III nitride compound semiconductor device, which is formed on a Group III nitride compound semiconductor substrate produced through a method for fabricating a Group III nitride compound semiconductor substrate as recited in any one of claims 1 through 6.

8. A Group III nitride compound semiconductor light-emitting device, which is produced by laminating a different Group III nitride compound semiconductor layer on a Group III nitride compound semiconductor substrate produced by a method for fabricating a Group III nitride compound semiconductor substrate as recited in any one of claims 1 through 6.

FIG. 1A

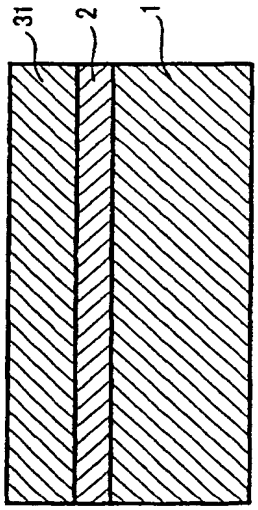


FIG. 1B

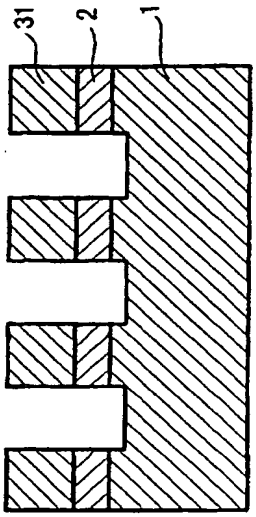


FIG. 1C

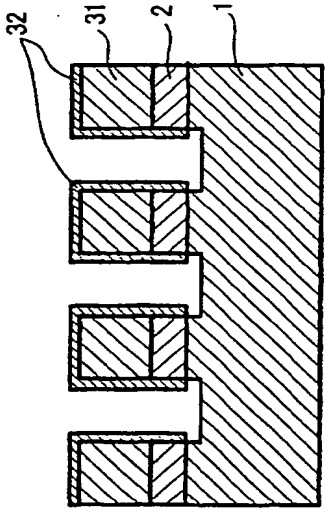
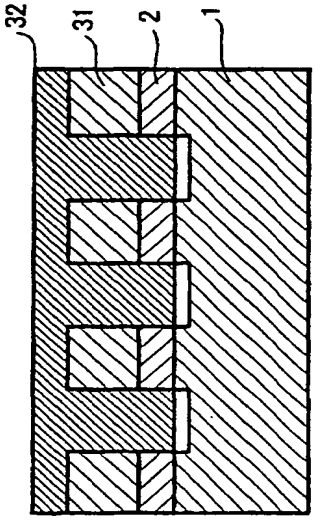


FIG. 1D



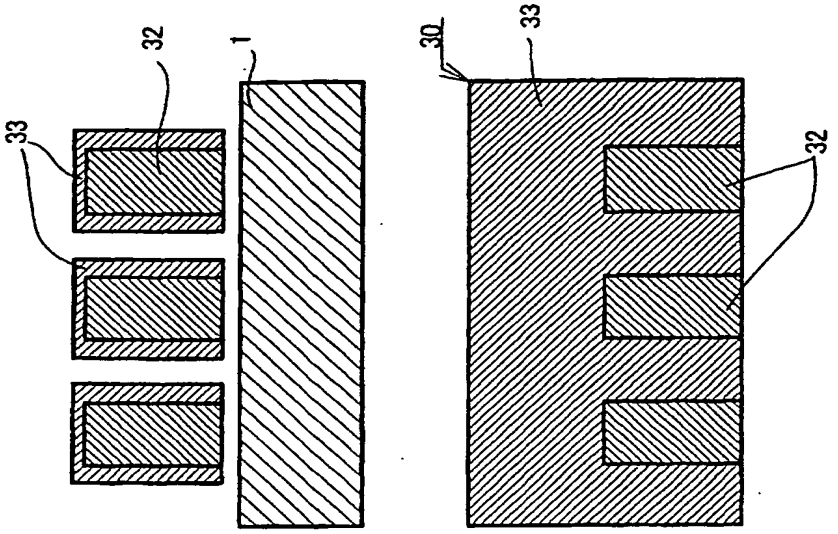


FIG. 2F

FIG. 2H

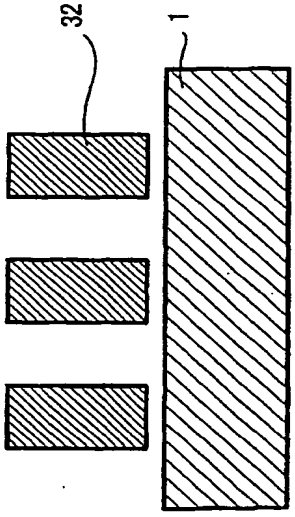


FIG. 2E

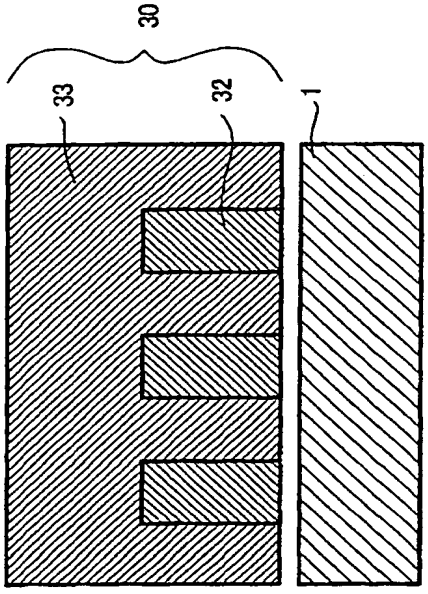


FIG. 2G

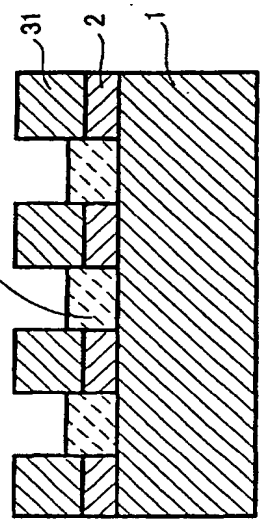


FIG. 3B

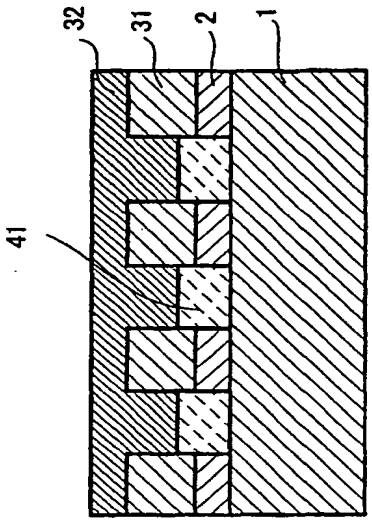


FIG. 3D

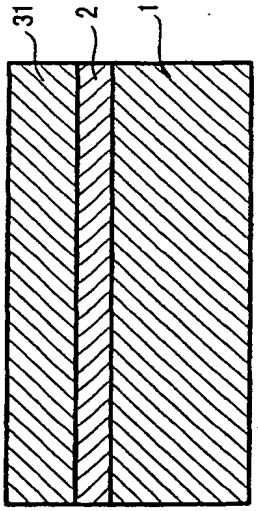


FIG. 3A

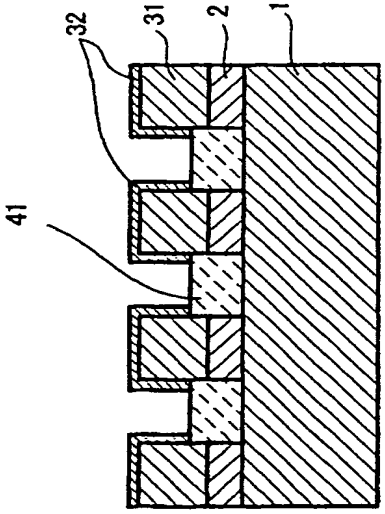


FIG. 3C

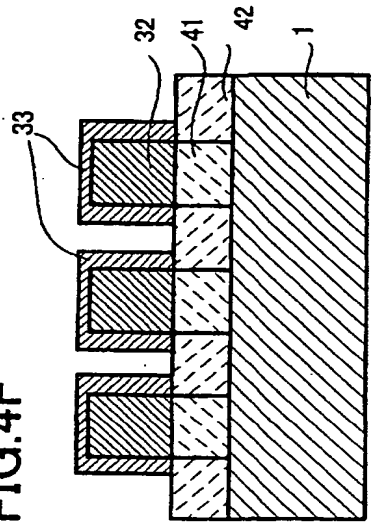


FIG.4F

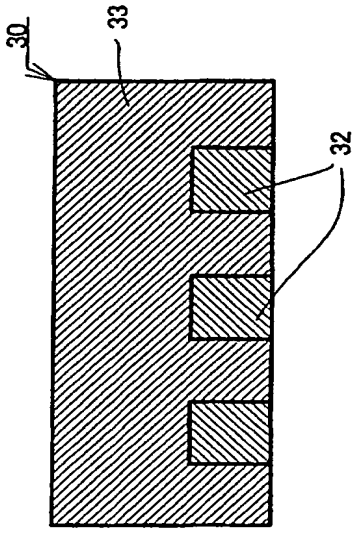


FIG. 4H

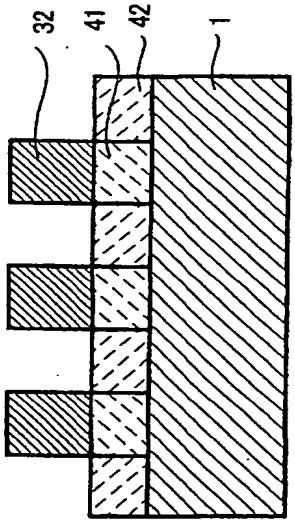


FIG. 4E

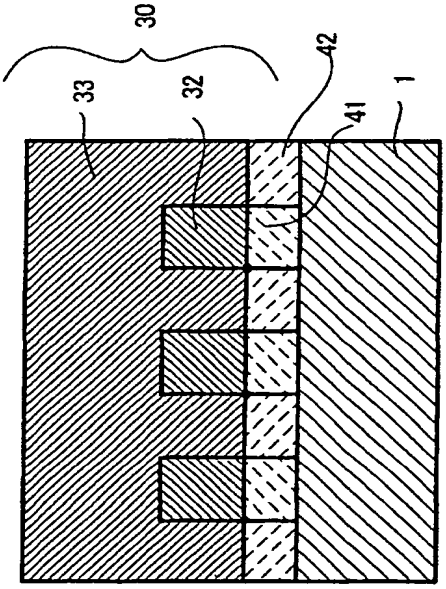


FIG. 4G

FIG. 5A

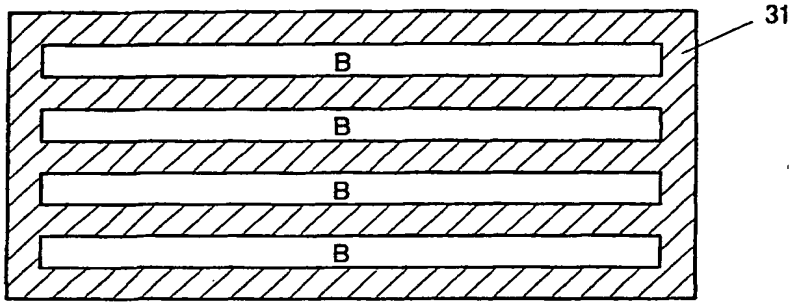


FIG. 5B

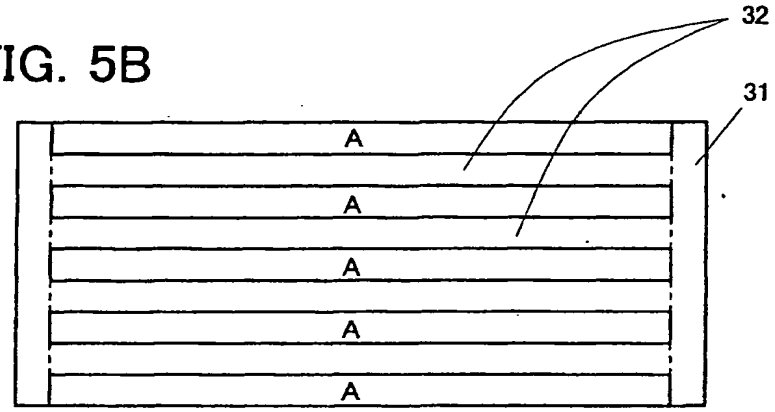


FIG. 5C

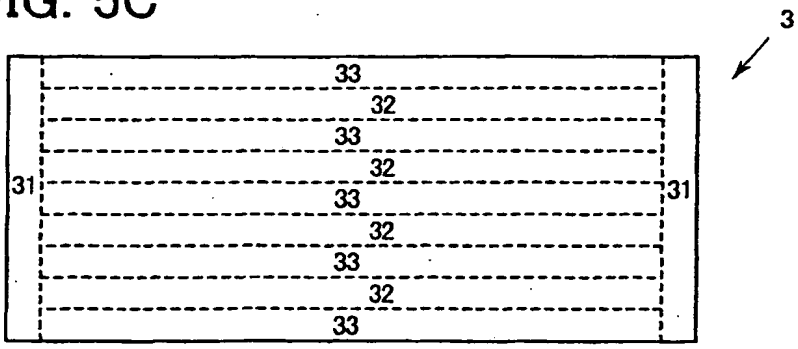


FIG. 6

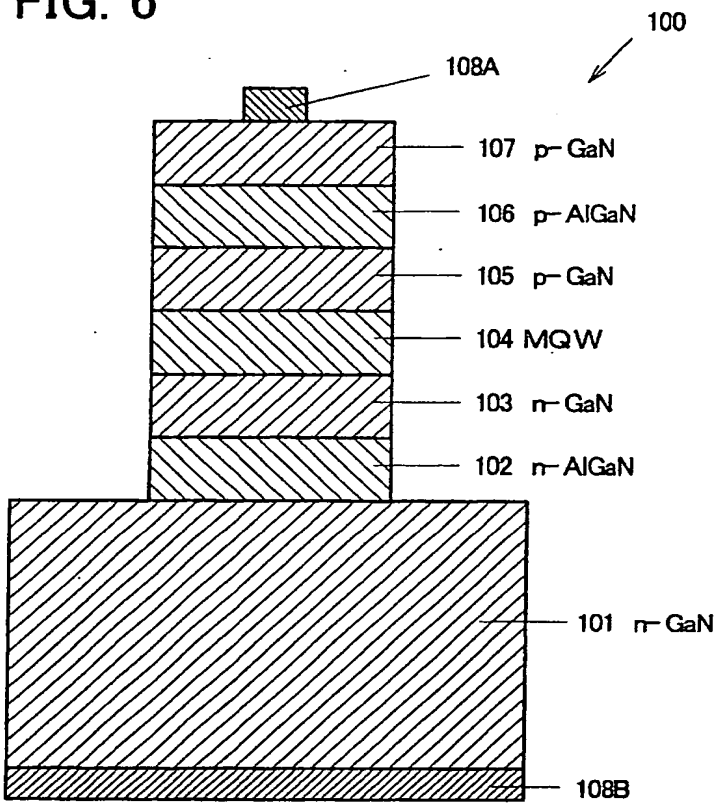
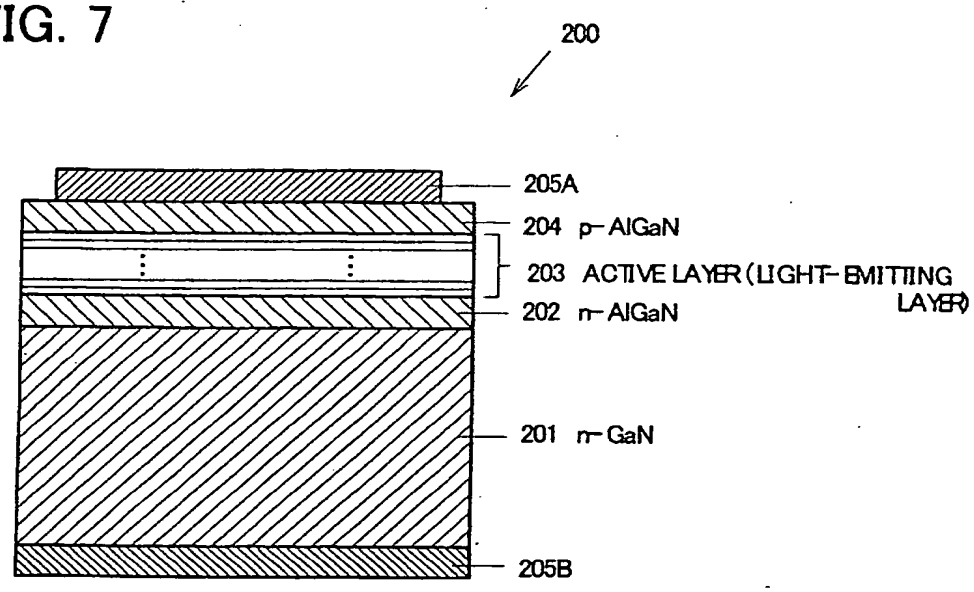

100
108A
107 p-GaN
106 p-AlGaN
105 p-GaN
104 MQW
103 n-GaN
102 n-AlGaN
101 n-GaN
108B

FIG. 7


200
205A
204 p-AlGaN
203 ACTIVE LAYER (LIGHT-EMITTING LAYER)
202 n-AlGaN
201 n-GaN
205B

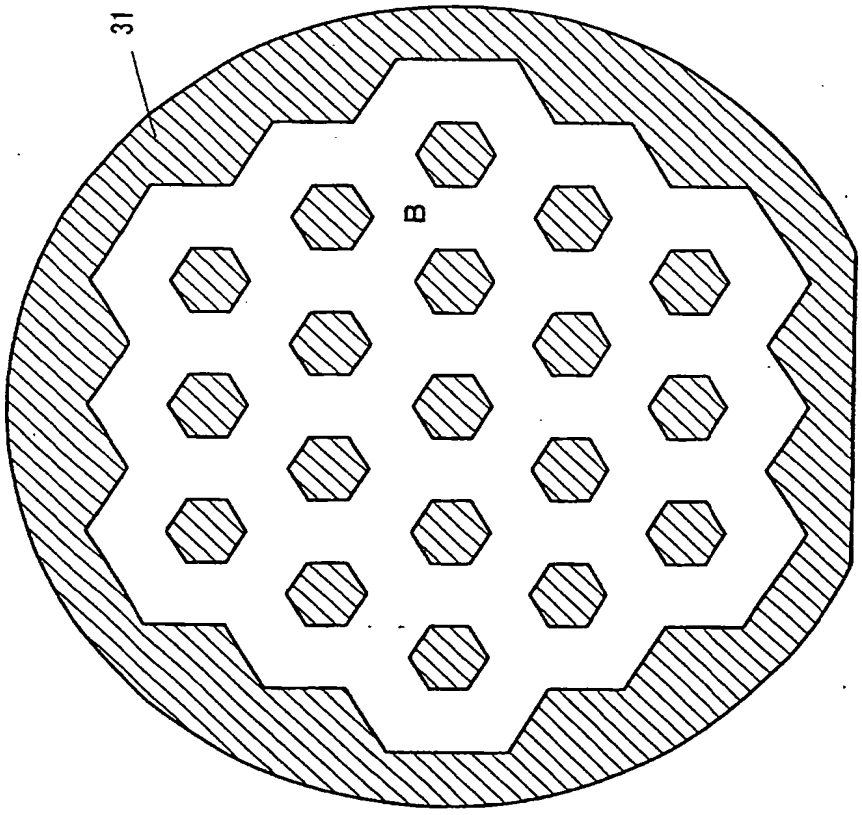


FIG. 8A

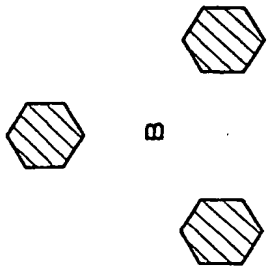
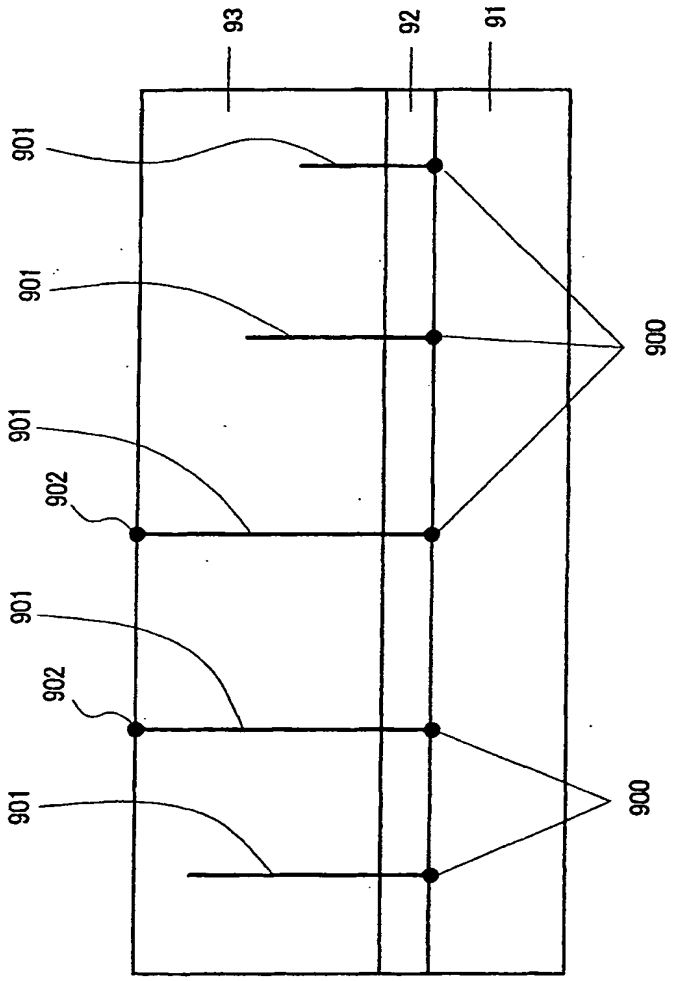


FIG. 8B

FIG. 9



INTERNATIONAL SEARCH REPORT

International application No.
PCT/JP01/01663

A. CLASSIFICATION OF SUBJECT MATTER
Int.Cl[7] H01L21/20, H01L21/205, H01L33/00, C30B29/38

According to International Patent Classification (IPC) or to both national classification and IPC

B. FIELDS SEARCHED

Minimum documentation searched (classification system followed by classification symbols)
Int.Cl[7] H01L21/20, H01L21/205, H01L33/00,

Documentation searched other than minimum documentation to the extent that such documents are included in the fields searched
Jitsuyo Shinan Koho 1922-1996 Toroku Jitsuyo Shinan Koho 1994-2001
Kokai Jitsuyo Shinan Koho 1971-2001 Jitsuyo Shinan Toroku Koho 1996-2001

Electronic data base consulted during the international search (name of data base and, where practicable, search terms used)

C. DOCUMENTS CONSIDERED TO BE RELEVANT

Category*	Citation of document, with indication, where appropriate, of the relevant passages	Relevant to claim No.
EY EA	JP, 2001-111174, A (Fuji Photo Film Co., Ltd.), 20 April, 2001 (20.04.01), Full text; Figs. 1 to 4 (Family: none)	1,4-8 2,3
EY EA	JP, 2001-122693, A (NEC Corporation), 08 May, 2001 (08.05.01), Full text; Figs. 1 to 15 (Family: none)	1,4-8 2,3

☐ Further documents are listed in the continuation of Box C. ☐ See patent family annex.

* Special categories of cited documents:
"A" document defining the general state of the art which is not considered to be of particular relevance
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"O" document referring to an oral disclosure, use, exhibition or other means
"P" document published prior to the international filing date but later than the priority date claimed
"T" later document published after the international filing date or priority date and not in conflict with the application but cited to understand the principle or theory underlying the invention
"X" document of particular relevance; the claimed invention cannot be considered novel or cannot be considered to involve an inventive step when the document is taken alone
"Y" document of particular relevance; the claimed invention cannot be considered to involve an inventive step when the document is combined with one or more other such documents, such combination being obvious to a person skilled in the art
"&" document member of the same patent family

Date of the actual completion of the international search	Date of mailing of the international search report
28 May, 2001 (28.05.01)	05 June, 2001 (05.06.01)
Name and mailing address of the ISA/ Japanese Patent Office	Authorized officer
Facsimile No.	Telephone No.

Form PCT/ISA/210 (second sheet) (July 1992)